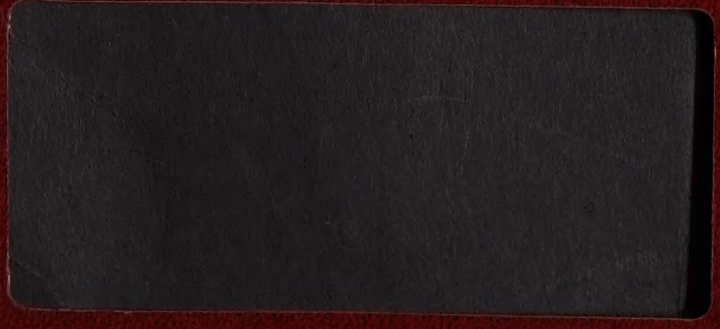
Instruction manual



DATA I/O

Programming systems for tomorrow... today

PROM PROGRAMMER
Program Card Set
909/919-1347-1

025-1347-1 REV E 4-80

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SOCKET ADAPTER

715-1311-2

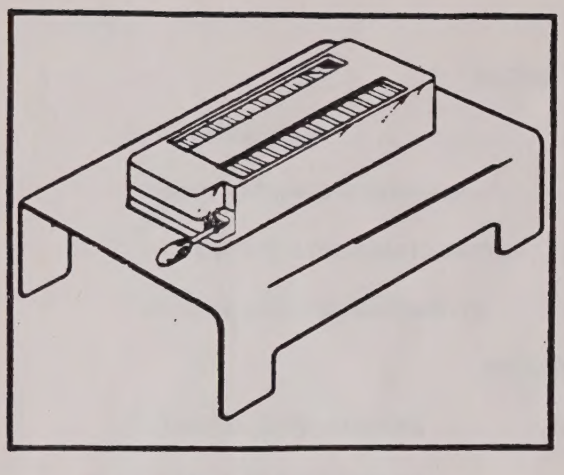


Figure 1. Socket Adapter 715-1311-2

A Socket Adapter consists of a zero insertion force socket with interface circuitry mounted on an adapter frame. It is used with a Data I/O programmer to match programmer electronics to PROM Memory pinout, byte size, and word limit requirements. Refer to the Data I/O Comparison Chart to match device configurations to Socket Adapter part numbers.

In use, the Socket Adapter is installed into a socket receptacle on the programmer front panel. The device to be programmed or read is inserted into the socket (with device pin 1 to upper left) and locked into place by means of a locking arm on the socket.

CAUTION

Do not switch programmer power while a device is installed in the Socket Adapter—voltage transients may cause spurious programming. Do not change devices when a programming operation is occurring (EXECUTE or START indicator illuminated).

STORAGE AND MAINTENANCE

The Socket Adapter should be stored in a location free of dust, excessive moisture, and extremes of temperature and humidity, assuring that top and bottom connectors are protected from possible physical damage.

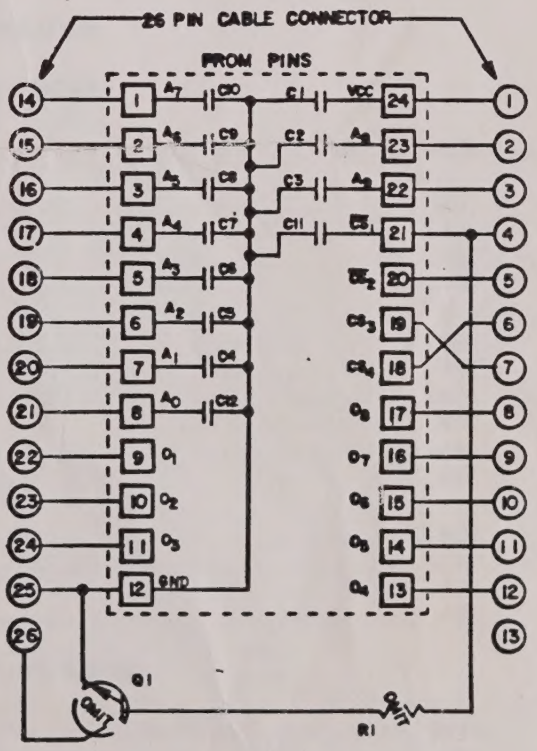
Periodically inspect each socket contact for accumulation of dirt and debris. Also inspect each contact for smooth opening and closing operation. Dirt and debris can usually be removed with compressed air.

The socket itself is constructed of a polysulfone material and should be cleaned only with methyl alcohol, freon TE, or detergent and water. Do not lubricate. If the socket fails in use, it is most probably caused by mechanical damage to the socket itself, which must be replaced in whole, as replacement parts are not available. Inspect each contact for opening and closing ability to ascertain when unit should be replaced.

CIRCUIT DESCRIPTION

Figure 2 is a schematic representation of Socket Adapter electronics. Device pinout is shown at the center. Socket pins, which mate with the programmer receptacle, are shown to either side. Looking at the top of the Socket Adapter, device pin one is on the upper left. Looking at the bottom of the Socket Adapter, connector pin one is on the upper left. Refer to the analog card schematic in the program card set Instruction Manual to determine signal routing to the connector pins from the analog card.

Some Socket Adapters utilize discrete components on the printed circuit board. Decoupling capacitors are used to isolate the address lines from certain high voltage transients which occur during programming. Word Limit Transistor Q1 is connected to saturate at device word limit, signalling the programmer on line CC to reverse the address count.



NOTES:
UNLESS OTHERWISE SPECIFIED
1. C1-C12 = .001/50V, 1w%

Figure 2. Schematic Diagram, Socket Adapter 715-1311-2

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2-1 Customer-Selectable Digital Card Jumpers

SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
INTEL				
256x4 FL	3621	VOL TS	16 PIN	1035-1
512x8 FL	3604A/AL	VOL OC	24 PIN	1318-1
512x8 FL	3624A	VOL TS	24 PIN	1318-1
512x8 FL	3604AL6	VOL OC	24 PIN	1318-2
1024x4 FL	3605A	VOL OC	18 PIN	1430
1024x4 FL	3625A	VOL TS	18 PIN	1430
1024x8 FL	3608	VOL OC	24 PIN	1311-1
1024x8 FL	3628	VOL TS	24 PIN	1311-1
2048x8 FL	3616	VOL OC	24 PIN	1311-2
2048x8 FL	3636	VOL TS	24 PIN	1311-2

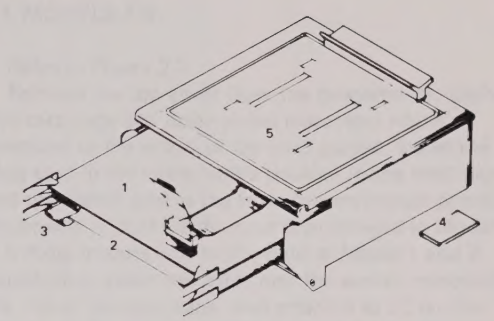
The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).

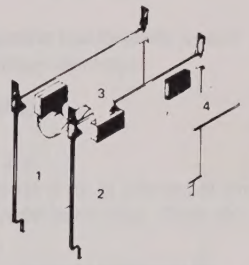
1.2 CALIBRATOR PROGRAM ADAPTER

The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD	701-1121
2. ANALOG CARD	701-1347-1
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1347-1
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

1.3 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer-Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP1	Abort Enable	B	—

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 and 2 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the

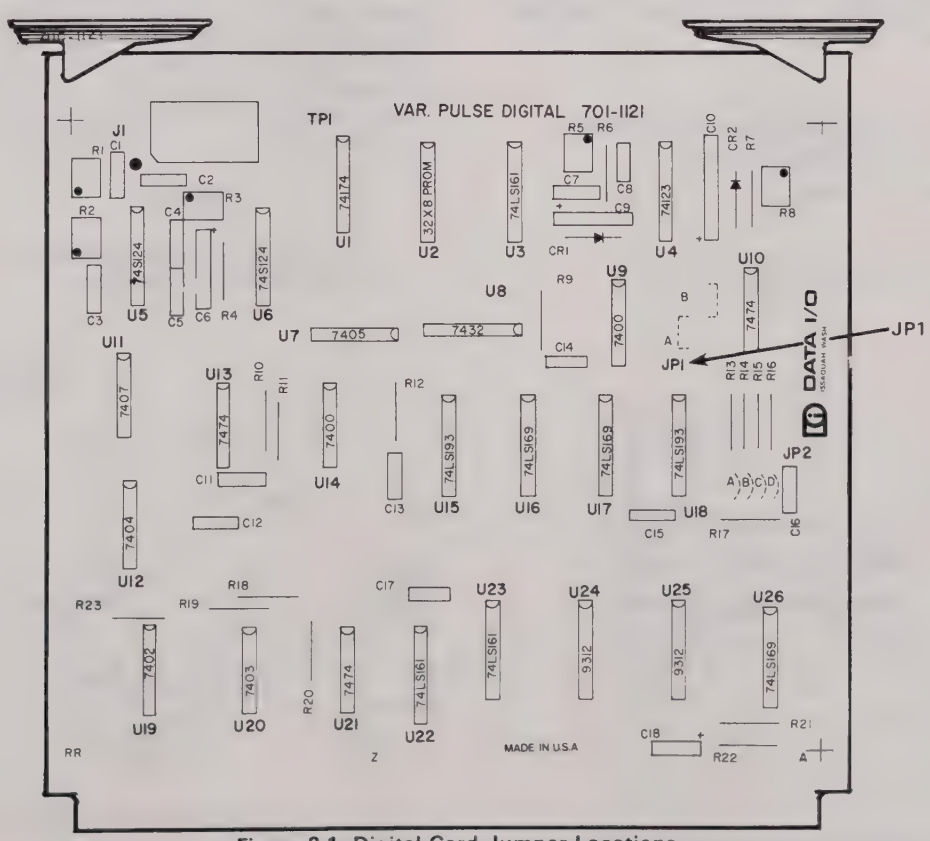


Figure 2-1. Digital Card Jumper Locations

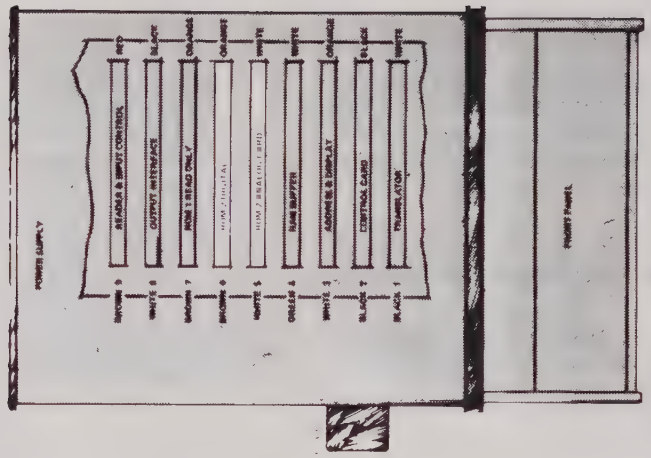


Figure 2-2. Installation of Card Set in Model 3 or 5

bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

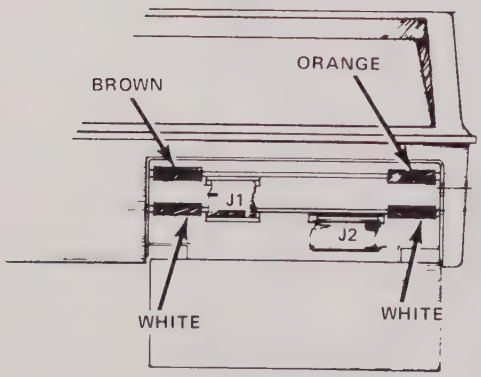


Figure 2-3. Installation of Card Set in Model 7 or 9

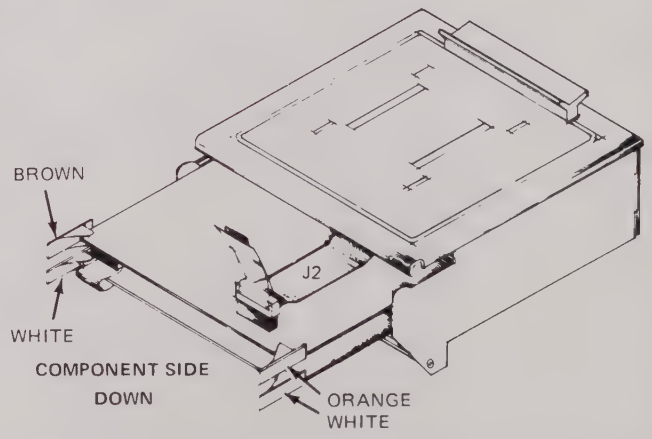


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics, its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

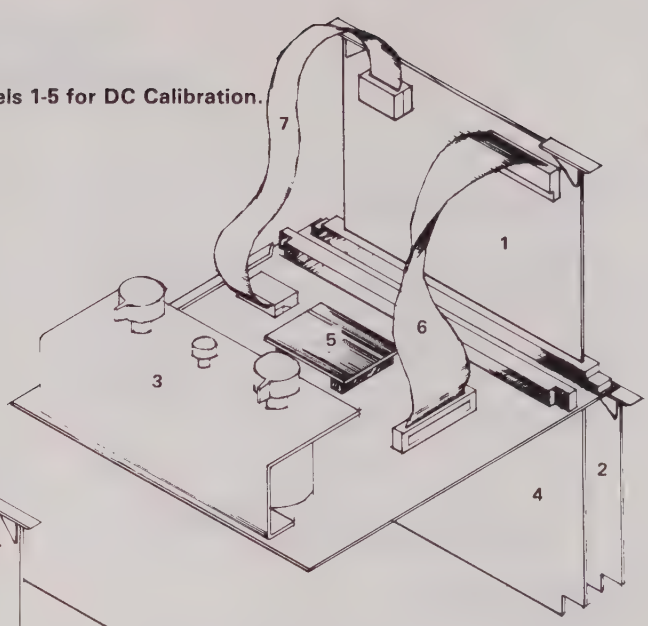
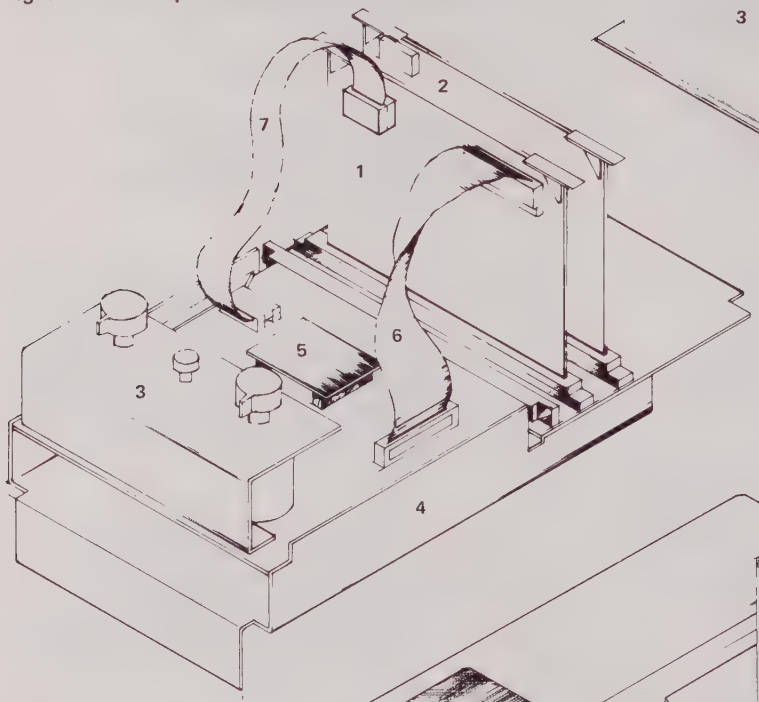


Figure 4-2. Set-up of Model 9 for DC Calibration.



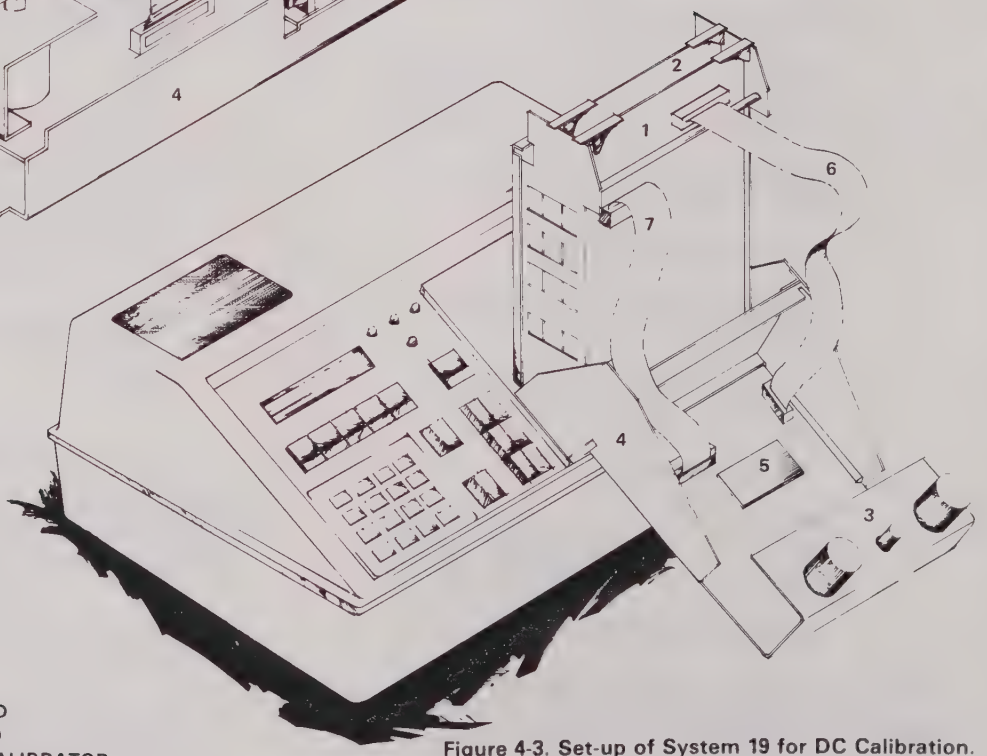


Figure 4-3. Set-up of System 19 for DC Calibration.

1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE
NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 919-XXXX part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE
To exit calibration, press:
SELECT
C0 (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

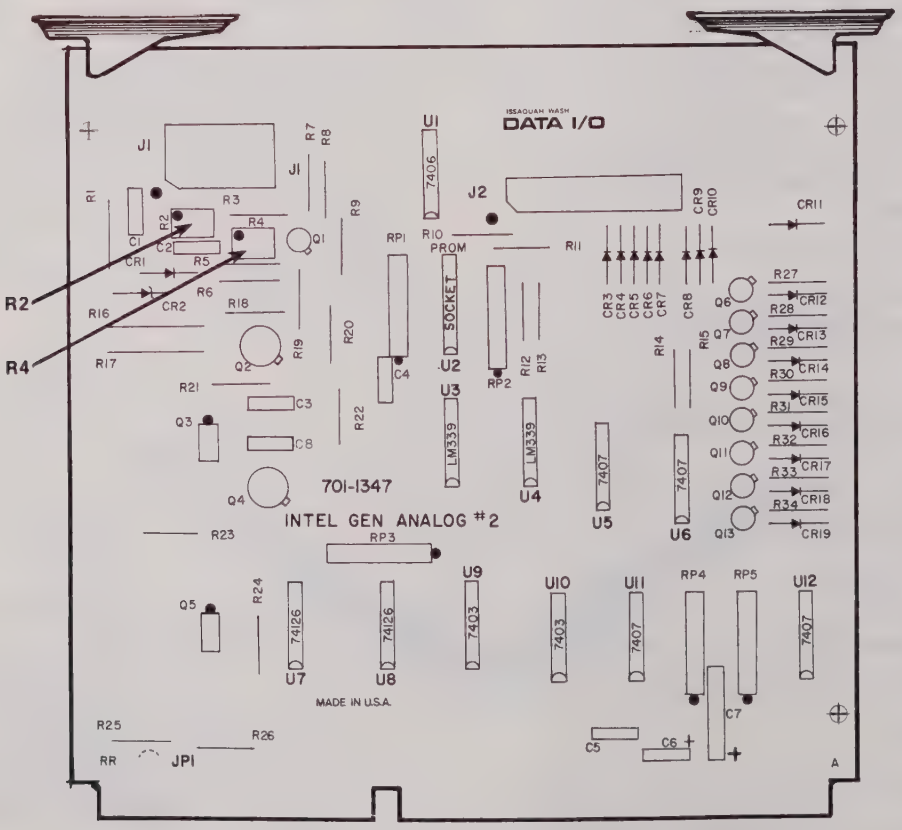


Figure 4-4. Analog Card Adjustment Locations

Calibration Chart

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CALIBRATION CHART 017-1347-1 | PROGRAM CARD 909-1347-1
FIXTURE 702-1071 | MANUFACTURER INTEL
PROGRAM ADAPTER 910-1347-1 | PROM INTEL GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
11-78	B	ECN #2565	FS	
4-25-80	B	ECN #3602	KJB	VSB

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
44	00	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments are located on the power supply board.
44	00	POWER +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	See programmer manual.
44	00	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15	
44	00	-9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8	
44	00	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V	R30	21.1	21.6	22.1	
44	00	VCC PROGRAM V SET (1)	2-1	001	01	001	5	1	TP3	R4	12.0	12.5	13.0	*Adjustment Step.*
44	00	VCC PROGRAM V REG	2-2	001	01	001	3	1	TP3		12.0		13.0	
44	00	VCC CURRENT ICC LIMIT	2-3	001	01	001	6	1	TP3		4.5		6.0	
44	02	VCC VERIFY V SET	2-4	002	02	002	5	1	TP3	R2	4.5	4.6	4.75	*Adjustment Step.*
4C	02	VCC READ LEVEL	2-5	003	03	003	5	1	TP3		4.75	5.0	5.25	
4C	02	VERIFY LOGIC LOW LEVEL	3-1	003	03	003	7	1	U3 P8		0.8		1.0	Set programmer in FWD. Test point located on
44	02	VERIFY LOGIC HIGH LEVEL	3-2	002	02	002	7	1	U3 P8		1.5		1.9	Set programmer in REV. analog card.
4C	02	$\overline{CE}$2 PROGRAM (2)	4-1	003	03	003	7	5	TP3		4.8		5.15	*Adjustment Step.*
44	01	$\overline{CE}$2 VERIFY	4-2	004	04	004	7	5	TP3		0.0		0.5	
44	01	$\overline{CE}$4. PROGRAM/VERIFY	4-3	004	04	004	3	7	TP3		6.0		8.0	
44	01	$\overline{CE}$4 READ (STOP)	4-4	004	04	004	7	7	TP3		4.0		5.0	Set programmer in STOP.
4C	00	CE3 READ	4-5	005	05	005	7	7	TP3		4.0		5.0	
4C	00	CE3 PROGRAM/VERIFY	4-6	005	05	005	7	6	TP3		4.8		5.15	
44	F8	BIT 8 PROGRAM I OUT	5-1	006	06	006	3	8	TP3		4.5		5.5	
44	F8	BIT 8 PROGRAM V CLAMP (3)	5-2	006	06	006	2	8	TP3		12.5		13.5	
44	D8	BIT 8 DESELECT	5-3	007	07	007	2	8	TP3		0.0		0.4	
44	D8	BIT 7 PROGRAM I OUT	5-4	007	07	007	3	9	TP3		4.5		5.5	
44	D8	BIT 7 PROGRAM V CLAMP (4)	5-5	007	07	007	2	9	TP3		12.5		13.5	
44	B8	BIT 7 DESELECT	5-6	008	08	010	2	9	TP3		00.0		0.4	
44	B8	BIT 6 PROGRAM I OUT	5-7	008	08	010	3	10	TP3		4.5		5.5	
44	B8	BIT 6 PROGRAM V CLAMP	5-8	008	08	010	2	10	TP3		12.5		13.5	
44	98	BIT 6 DESELECT	5-9	009	09	011	2	10	TP3		0.0		0.4	
44	98	BIT 5 PROGRAM I OUT	5-10	009	09	011	3	11	TP3		4.5		5.5	
44	98	BIT 5 PROGRAM V CLAMP	5-11	009	09	011	2	11	TP3		12.5		13.5	

COMMENTS

Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENTS below.

- Switch S1 must be depressed for accurate readings.
- CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CALIBRATION CHART 017-1347-1

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U	U	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
41	78	BIT 5 DESELECT	5-12	010	0A	012	2	11	TP3		0.0		0.4
41	78	BIT 4 PROGRAM I OUT	5-13	010	0A	012	3	12	TP3		4.5		5.5
41	78	BIT 4 PROGRAM V CLAMP	5-14	010	0A	012	2	12	TP3		12.5		13.5
41	58	BIT 4 DESELECT	5-15	011	0B	013	2	12	TP3		0.0		0.4
41	58	BIT 3 PROGRAM I OUT	5-16	011	0B	013	3	23	TP3		4.5		5.5
41	58	BIT 3 PROGRAM V CLAMP	5-17	011	0B	013	2	23	TP3		12.5		13.5
41	38	BIT 3 DESELECT	5-18	012	0C	014	2	23	TP3		0.0		0.4
41	38	BIT 2 PROGRAM I OUT	5-19	012	0C	014	3	22	TP3		4.5		5.5
41	38	BIT 2 PROGRAM V CLAMP	5-20	012	0C	014	2	22	TP3		12.5		13.5
441	18	BIT 2 DESELECT	5-21	013	0D	015	2	22	TP3		0.0		0.4
44	18	BIT 1 PROGRAM I OUT	5-22	013	0D	015	3	21	TP3		4.5		5.5
44	18	BIT 1 PROGRAM V CLAMP	5-23	013	0D	015	2	21	TP3		12.5		13.5
44	F8	BIT 1 DESELECT	5-24	014	0E	016	2	21	TP3		0.0		0.4
44	00	DI BUS (BIT CONTROL)	5-25	015	0F	017	3	8, 10,	TP3		0.0		0.4
44	00							12,22,	TP3		0.0		0.4
44	00							9, 11,	TP3		4.5		5.5
44	00							23,21	TP3		4.5		5.5
44	00	DI BUS (BIT CONTROL)	5-26	015	0F	017	3	8, 10,	TP3		4.5		5.5
44	00							12,22,	TP3		4.5		5.5
44	00							9, 11,	TP3		0.0		0.4
44	00							23,21	TP3		0.0		0.4
C4	0A	BIT 8 COMPARATOR TEST	6-1	016	10	020	5	8					
C4	0A	BIT 7 COMPARATOR TEST	6-2	016	10	020	5	9					
C4	0A	BIT 6 COMPARATOR TEST	6-3	016	10	020	5	10					
C4	0A	BIT 5 COMPARATOR TEST	6-4	016	10	020	5	11					
C4	0A	BIT 4 COMPARATOR TEST	6-5	016	10	020	5	12					
C4	0A	BIT 3 COMPARATOR TEST	6-6	016	10	020	5	23					
C4	0A	BIT 2 COMPARATOR TEST	6-7	016	10	020	5	22					
C4	0A	BIT 1 COMPARATOR TEST	6-8	016	10	020	5	21					

	MOD 5	9	19	
LOAD	BITS 1,3,5,7 ON	55	55	DI Bus
LOAD	BITS 2,4,6,8 ON	AA	AA	DI Bus
CONFIRM	BIT 8 ON	7F	7F	DO Bus
CONFIRM	BIT 7 ON	BF	BF	DO Bus
CONFIRM	BIT 6 ON	DF	DF	DO Bus
CONFIRM	BIT 5 ON	EF	EF	DO Bus
CONFIRM	BIT 4 ON	F7	F7	DO Bus
CONFIRM	BIT 3 ON	FB	FB	DO Bus
CONFIRM	BIT 2 ON	FD	FD	DO Bus
CONFIRM	BIT 1 ON	~~EF~~	EF	DO Bus

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
44	78	ADDRESS TEST VIL (5)	7-1	682	2AA	1252	7	20	TP3		0.0		0.4
44	78	ADDRESS TEST VIH	7-2	682	2AA	1252	7	19	TP3		4.8		5.15
44	78	ADDRESS TEST VIL	7-3	682	2AA	1252	7	18	TP3		0.0		0.4
44	78	ADDRESS TEST VIH	7-4	682	2AA	1252	7	17	TP3		4.8		5.15
44	78	ADDRESS TEST VIL	7-5	682	2AA	1252	7	16	TP3		0.0		0.4
44	78	ADDRESS TEST VIH	7-6	682	2AA	1252	7	15	TP3		4.8		5.15
44	78	ADDRESS TEST VIL	7-7	682	2AA	1252	7	14	TP3		0.0		0.4
44	78	ADDRESS TEST VIH	7-8	682	2AA	1252	7	13	TP3		4.8		5.15
44	78	ADDRESS TEST VIL	7-9	682	2AA	1252	7	2	TP3		0.0		0.4
44	78	ADDRESS TEST VIH	7-10	682	2AA	1252	7	3	TP3		4.8		5.15
44	78	ADDRESS TEST VIL	7-11	682	2AA	1252	7	4	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-12	1365	555	2525	7	20	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	7-13	1365	555	2525	7	19	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-14	1365	555	2525	7	18	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	7-15	1365	555	2525	7	17	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-16	1365	555	2525	7	16	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	7-17	1365	555	2525	7	15	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-18	1365	555	2525	7	14	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	7-19	1365	555	2525	7	13	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-20	1365	555	2525	7	2	TP3		4.8		5.15
44	00	ADDRESS TEST VIL	7-21	1365	555	2525	7	3	TP3		0.0		0.4
44	00	ADDRESS TEST VIH	7-22	1365	555	2525	7	4	TP3		4.8		5.15
44	00	GROUND TEST	8-1	1365	555	2525	8	24	TP3		0.0		0.08
44	00	← DATA PATTERN FOR ALL WORDS NOT SHOWN											

CALIBRATION CHART 017-1347-1

NOTES:

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 — 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 — 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5:	Observe the START and STOP indicators.
Model 9:	Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.
System 19:	Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5:	Press the START/STOP key.
Model 9:	a. Press KEYBOARD to stop.
	b. Press EXECUTE to start.
System 19:	a. To set the programmer in START, press KEYBD, ENTER and START.
	b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5:	Press the FWD key or the REV key.
Model 9:	See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.
Revision "A" Software:	Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:
	a. Ground J1-16 on the analog card.
	b. Press LOAD.
	c. Press EXECUTE.
	d. Press KEYBOARD.
	e. Key in data — Ø hex — at address ØØ1.
	f. Press VERIFY.
	g. Press EXECUTE. The programmer will mis-verify

at the address containing data and will STOP in FWD.

h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.)

Revision "A" Software: Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in the Model 9 hex data called out on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software: With the KEYBOARD indicator illuminated and all the others OFF, use the hex keypad to key in the Model 9 hex data called out on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the System 19 hex data into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5: Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF.

Model 9: With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19: With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Remove the digital card from the card slot.

c. Check the Timing Diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

d. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

e. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

f. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the Timing Diagram. Connect an input probe to TP3 on the calibrator.

g. Reinstall the digital card in the slot from which it was removed.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1—5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the Timing Diagram specifies the correct polarity. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1—5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data at several addresses. Enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets. Return to address Ø.

4. Select the PROGRAM mode:

Models 1—5, press:	RESET PROGRAM AUTO RAM-ROM2

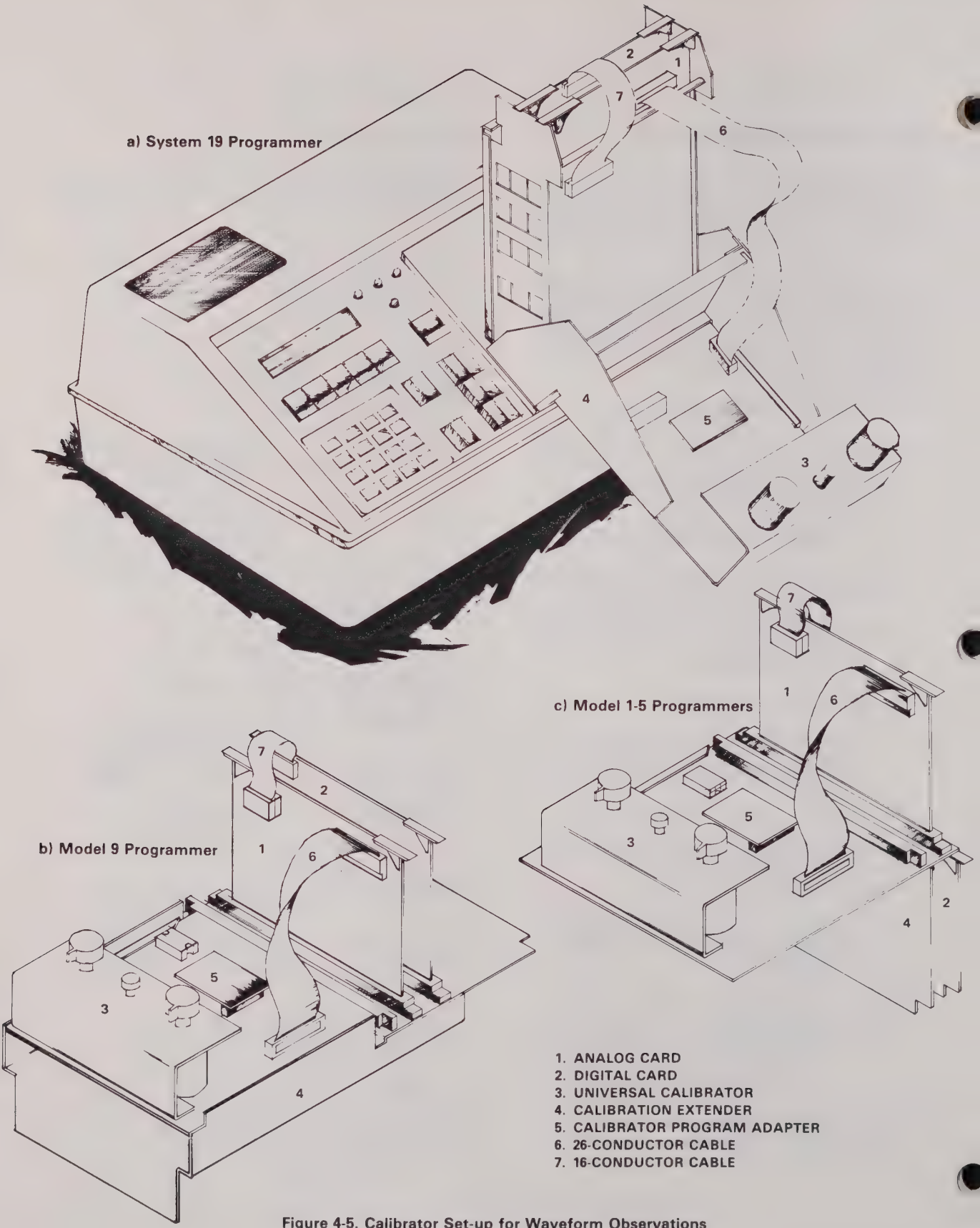
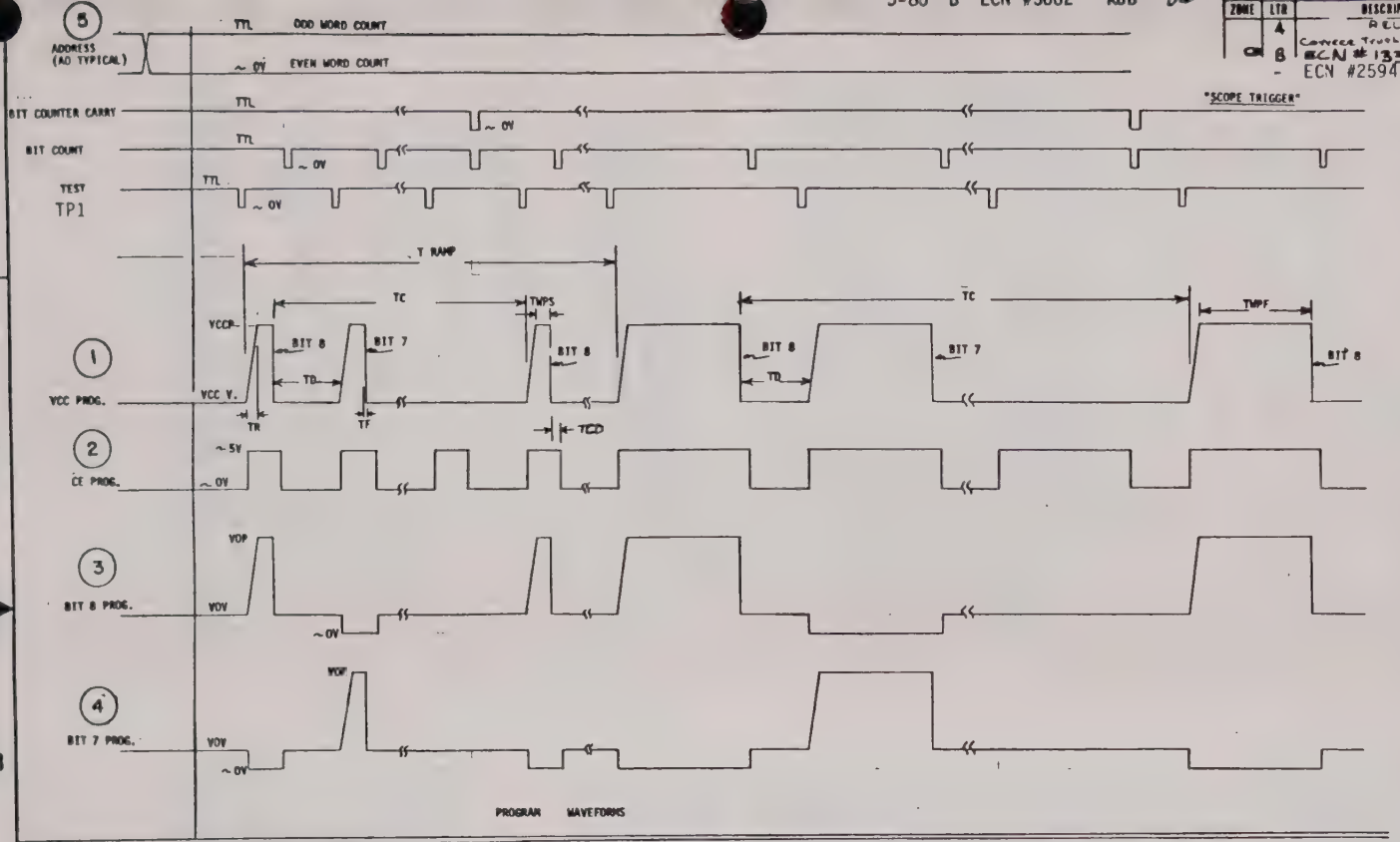


Figure 4-5. Calibrator Set-up for Waveform Observations

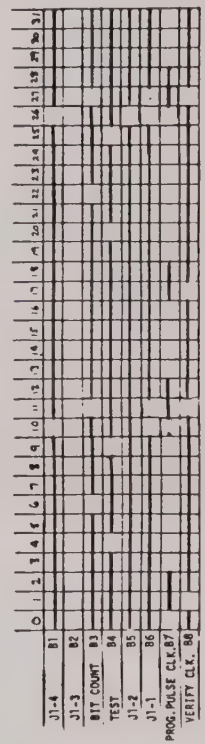
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE	4-11-77	GJ
	B	Correct Truth Table ECN # 1333 - ECN #2594	5/6/77 11-78	GJ FS



TRUTH TABLE

LINE = HI(1); NO LINE=LOW (0)

TIMING ROM U2



NOTES:

DIGITAL CARD JUMPERS

JP1 = B

JP2A = SHORT

JP2B = OPEN

JP2C = SHORT

JP2D = SHORT

INITIAL PULSE WIDTH (TWPS) = 200 ns

ABORT TIMER

800 MS ± 20%

OVERPROGRAM

128 CYCLES FOLLOWED BY A 2.5 ± 0.3 ms PULSE TO ALL OUTPUTS TO BE PROGRAMMED.

WAVEFORM VARIABLES

TD = 1.8 us Nom.
1.5 us Min.

TC = 10 us Min.

TCD = 100 ns Min.

TR = 400 ± 100 ns.

TF = 100 + 100 ns. - 50 ns

TWPS = 200 ± 40 ns.

TWPF = 8.0 ± 0.8 us.

T RAMP = 180 ± 20 MS 4/BIT
360 ± 40 MS 8/BIT

VCCV = 4.6 ± 0.10 V.

VCCP = 12.5 ± 0.5 V.

VOP ~ 13 V.

VOV ~ 5.2 V.

For calibration, the card set polarity defaults to VOL.

These waveforms correspond to callouts on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.

TOLERANCES (EXCEPT AS NOTED)	DATA I/O	
DECIMAL ±	TITLE: TIMING DIAGRAM INTEL GENERIC NO 2	
ANGULAR ±		
DRAWN BY: GJ	SIZE: C	CODE IDENT NO: DRAWING NO. 007-1347-1
APPROVED BY: GJ	SCALE	SHEET

A 3/78

Model 9, press:	PROGRAM
System 19, press:	SELECT C1 START PROG

5. Initiate waveforms:

Models 1—5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1—5 and 9, press:	STOP
System 19, press	KEYBD

4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

CAUTION

The reject jumper must be reinstalled. Otherwise, the device's programming specifications will be violated, and the programmer and/or cardset may be damaged by a prolonged attempt to program a defective device.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Ground J1-16.
6. With the Universal Calibrator switches set to observe CE Program, connect the scope probe to TP3 on the Universal Calibrator. Trigger the scope on TP3.
7. Repeat the key sequence in the Waveform Test Procedure, 4.4.2 steps 1-5. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort function of the digital card is operative. The System 19 will display Error 22.

NOTE

The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated.

However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram contact your nearest Data I/O Service Representative for calibration information.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

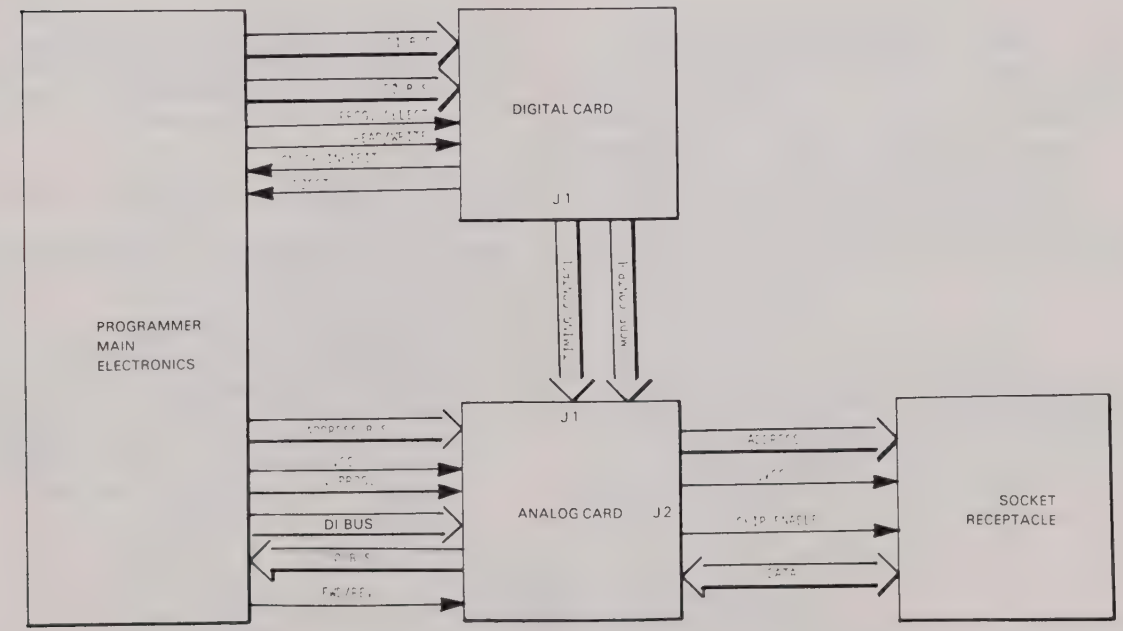


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

The basic programming cycle is handled by the digital card. As the desired address is selected, machine control is transferred to the digital card and the required bits are programmed. Control is then transferred back to the programmer and a verification is performed. The address is incremented and the cycle is repeated.

Figure 5-2 gives a generalized block diagram of the variable-pulse digital card. This diagram shows signal flow and functional relationships between the blocks but does not include detailed interconnection information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.1 PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set upon receiving a Write command on line AA. This causes the digital card to begin operation. All counters, memories and timers except the Pulse Counter are initialized before the Program Memory is set.

5.2.2 CLOCK GENERATION

The variable-pulse digital card has a three-clock timing scheme provided by the Sequence Clock, Program Pulse Clock and Ramp Clock. Prior to setting of the Program Memory, the Sequence Clock is running while the Program Pulse Clock and Ramp Clock are stopped. When the Program Memory sets, the Sequence Counter is enabled, its clock is left running and the other two clocks are stopped.

5.2.3 SEQUENCE GENERATOR

The Sequence Generator consists of a 4-bit counter, a 32x8 timing ROM and a 6-bit register. The combination generates timing signals for analog card control, along with bit test, bit increment, program pulse and sequence clock control.

The first command generated activates the Program Pulse Clock. This enables synchronous loading of Ramp-Counter data into the Pulse Counter. The Ramp Counter is loaded to the value determined by JP2 before the Program Memory is set.

The second command is bit test, which gates the compared DI and DO Bus Decoder outputs, supplying a decision whether there is a bit to program. Bit increment follows bit test.

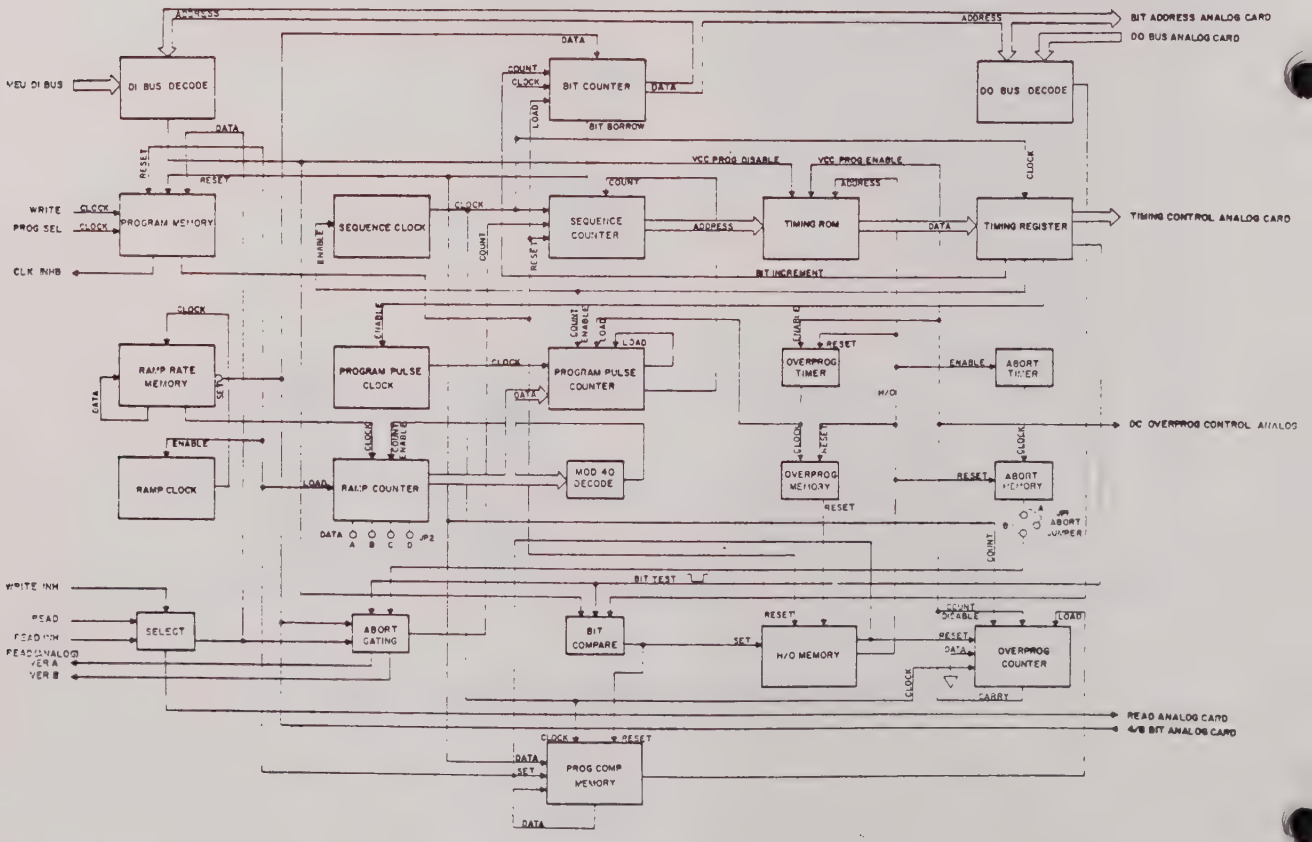


Figure 5-2. Block Diagram, 1121 Digital Card

5.2.4 BIT COUNTER

The Bit Counter counts bit-increment pulses arriving from the Timing Register. The Bit Counter counts down from either 3 or 7, as determined by 4/8 Bit mode input from the Analog Card. Outputs from the Bit Counter address the DO and DI Bus Decoders and are supplied as bit addresses to the analog card. When the Bit Counter reaches zero, its borrow pulse resets the Program Complete Memory when in high order, and resets the Program Memory when in low order.

5.2.5 H/O MEMORY AND PULSE COUNTER

Following bit increment, the sequencer loops back to bit test. If bit test yields a bit to program, the High Order Memory Sets, addressing the timing ROM into high order (H/O). The sequencer advances to Program stopping the Verify Clock and starting the Program Pulse Clock. The sequencer remains in Program until the Pulse Counter counts down and clocks it off Program. The third Pulse Counter borrow loads the current Ramp Counter output into the Pulse Counter. Then the Sequence Clock restarts and the sequencer advances to the high order bit test.

If bit test still yields a bit to program, the sequencer repeats another program-bit test sequence. This sequence repeats as long as bit test yields a bit to program and the Abort Timer has not timed out.

5.2.6 RAMP COUNTER

The Ramp Counter is advanced by the Ramp Clock to generate data for the Pulse Counter after the H/O Memory is set.

The Ramp Counter in conjunction with the Pulse Counter generates the increasing program pulse width. The initial width, the beginning count of the Ramp Counter, is determined by JP2. The final width is obtained when the Ramp Counter reaches a count of 40. The clock rate times the Counter value (40 minus the JP2 value) equals the specified ramp time.

5.2.7 PROGRAM COMPLETE MEMORY

When bit test yields a bit to program, the Program Complete Memory sets. This memory resets on carry from the Bit Counter. Therefore, if no bit to program decision is made this memory never sets, signaling that all bits have programmed.

5.2.8 OVERPROGRAM COUNTER

With the Program Complete Memory reset, the Overprogram Counter will increment with each Bit Counter carry. The sequencer will output signals enabling serial program pulses for all bits to program. Overprogram pulses are applied until the counter reaches the overprogram value.

5.2.9 OVERPROGRAM TIMER

When the Overprogram Counter reaches its limit the Overprogram Timer is started. When this timer is on, the Program Pulse Counter is held loaded, keeping the sequencer in Program, applying program levels to all bits to be programmed. When the timer times out, the load line is released on the Pulse Counter and the counter counts down, clocking the sequencer out of Program and setting the Overprogram Memory. On the next bit test the H/O Memory is reset addressing the Sequencer ROM back into low order. The Ramp and Overprogram Counters are reloaded, the Abort and Overprogram Timers are reset and the Abort and Overprogram Memories are cleared. The sequencer advances to bit increment, resetting the program memory. The sequence is then repeated for the next word.

5.2.10 ABORT TIMER

The Abort Timer measures the time required to program a bit when JP1 is in Position B. If programming time is excessive the Abort Memory sets, signaling a reject, and the sequencer is halted. The Abort Timer output is gated with bit test such that an abort is possible only during high order bit test.

5.3 ANALOG CARD

The 1347-1 analog card provides the bias supplies, drive capability and sense amplifiers needed to program and read the Intel generic family of PROMs, when used in conjunction with the variable-pulse digital card. Refer to Figure 5-3.

5.3.1 ADDRESS DRIVERS

Address signals from the address bus are buffered by open-collector devices (U11, U12) where outputs are pulled up to 5 V. These outputs are connected to the device through J2 and a ribbon cable to the device socket assembly.

5.3.2 Vcc SUPPLY

The Vcc supply is operated from the machine's programable supply which is adjusted to 21.6 V by the voltage select resistors, R25 and R26. Q2, Q3, R17 and the 5.6 volt reference diode (CR2) perform the current limiting function. Transistors Q4 and Q5 form a unity gain feedback amplifier. The Program voltage level is obtained from the voltage divider action of R4 and R6. The Read voltage level is obtained when a high signal from digital card J1 pin 2 causes U1 pin 8 to short R2 to ground. The input voltage to the unity gain amplifier is now determined by the divider action of R6 and R2. The effect of R4 is omitted due to the back-biasing of diode CR1. Another Read Vcc level is obtained when the cardset is not selected as an output. J1 12 goes high causing Q1 to turn on. This parallels R3 with R6 causing the voltage to increase.

5.3.3 BIT DECODER

The Bit Decoder (U2) is a 32x8 ROM which receives its input from the Bit Counter on the digital card. Refer to the Truth Table at the back of this manual for the specific decode matrix.

5.3.4 PROGRAM ENABLE DRIVERS

The Program Enable Drivers consist of drivers U5 and U6. Each driver output is connected to a 5 mA current source and to the device bit line through diodes CR3 to CR10. The 5 mA current sources consist of Q6 through Q3 and R27 through R34 with CR2 providing the reference voltage. CR12 through CR19 and CR11 clamp the current sources to a maximum of Vcc plus two diode drops. Unselected bits are held low during the program cycle, while the selected bit is fed 5 mA. Two 7403 devices U9 and U10 are wire-ORed with the bit decoder outputs such that

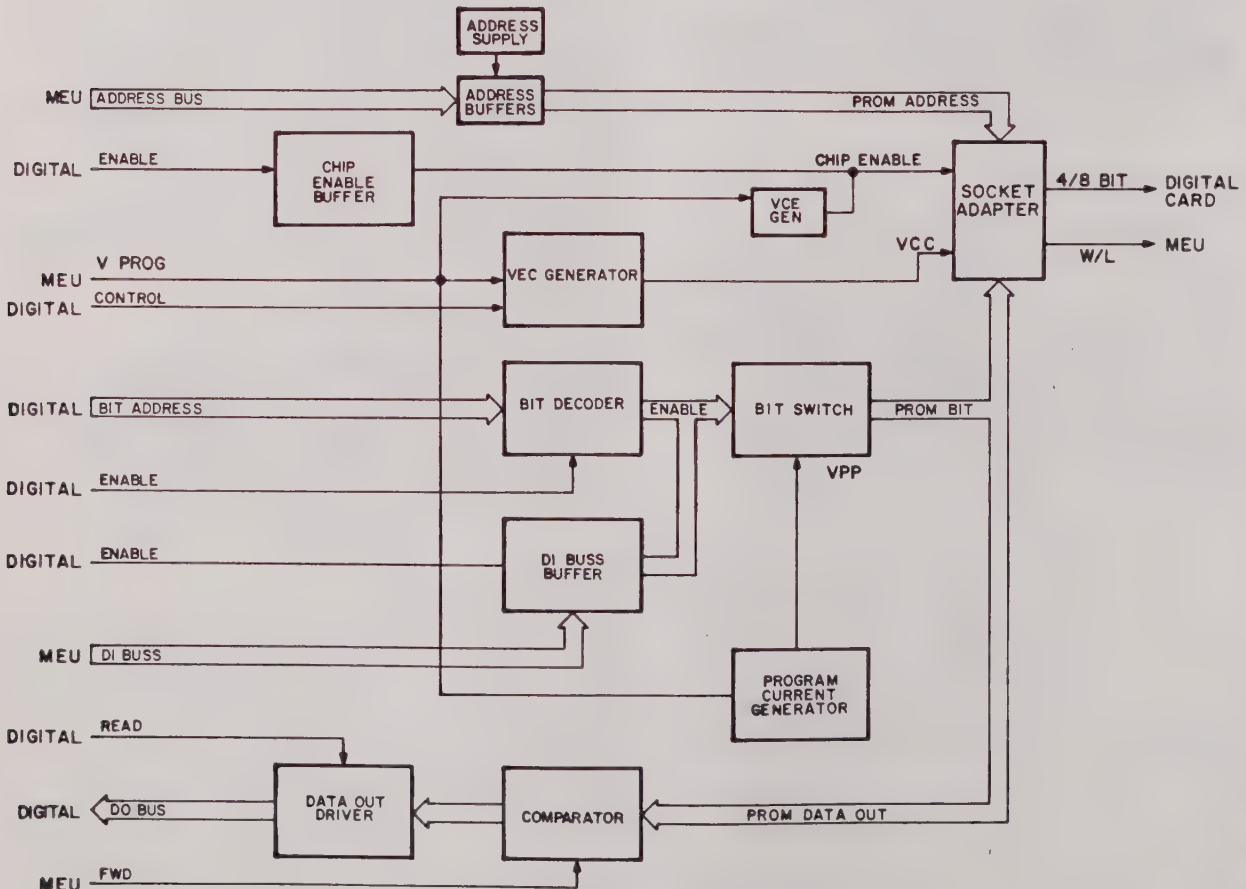


Figure 5-3. Analog Card Block Diagram

both outputs must be high to enable the 5 mA. These gates are enabled during Program and are disabled during Verify and Read via J1-4.

Two comparators, U3 and U4, sense the output levels. The 5 mA current sources are used as a pull-up for open collector devices. The reference voltage is developed by divider R9, R20 and R22. Pin 12 of U1 grounds R9, decreasing the compare level when the machine FWD line goes high. This provides separate VOL and VOH compare levels.

5.3.5 READ OUT GATES

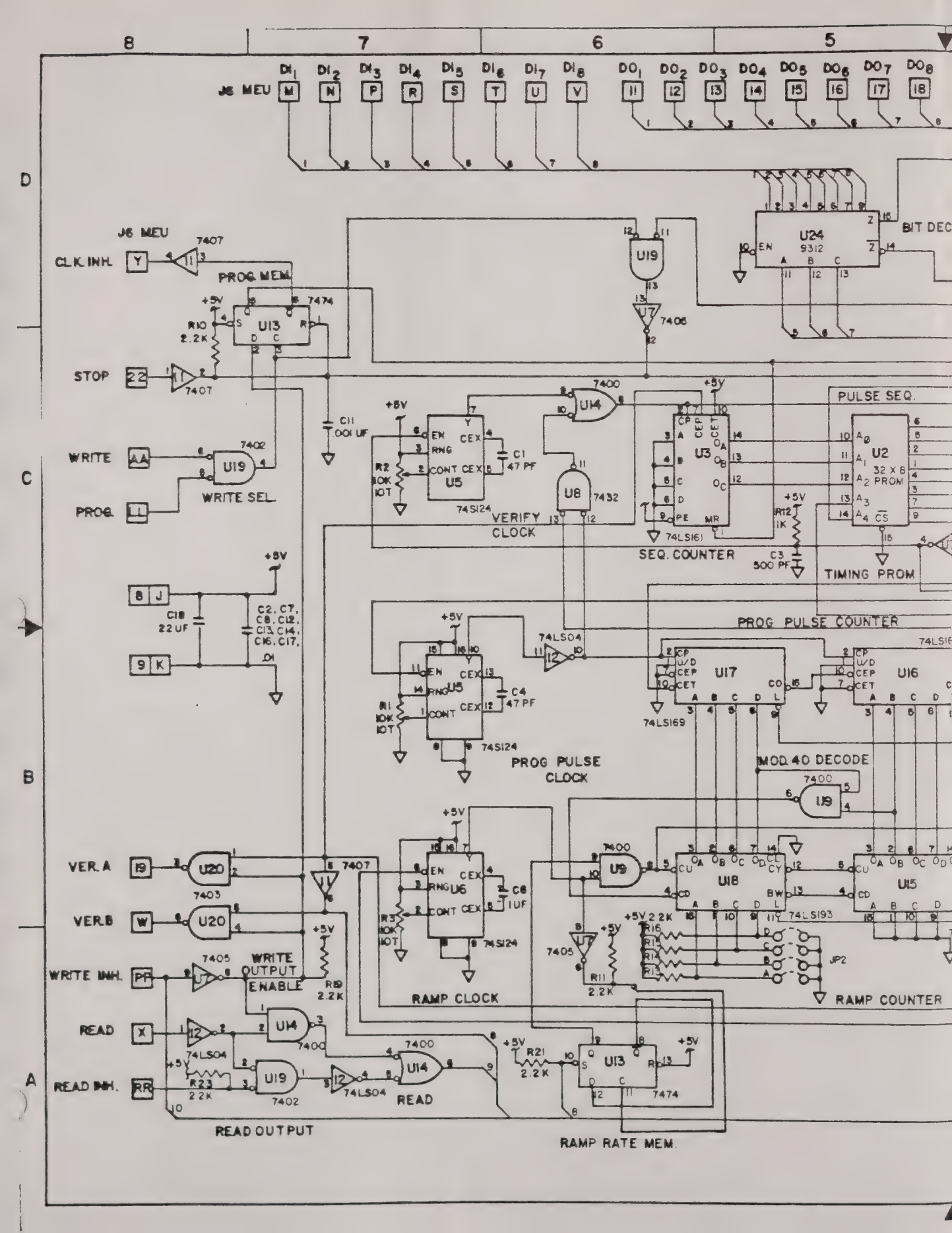
The outputs of the Data Comparators are fed to U7 and U8. When the devices are enabled by pin 16 of J1 from the digital card, the output from the Data Comparators is transferred to the machine Output Data Bus.

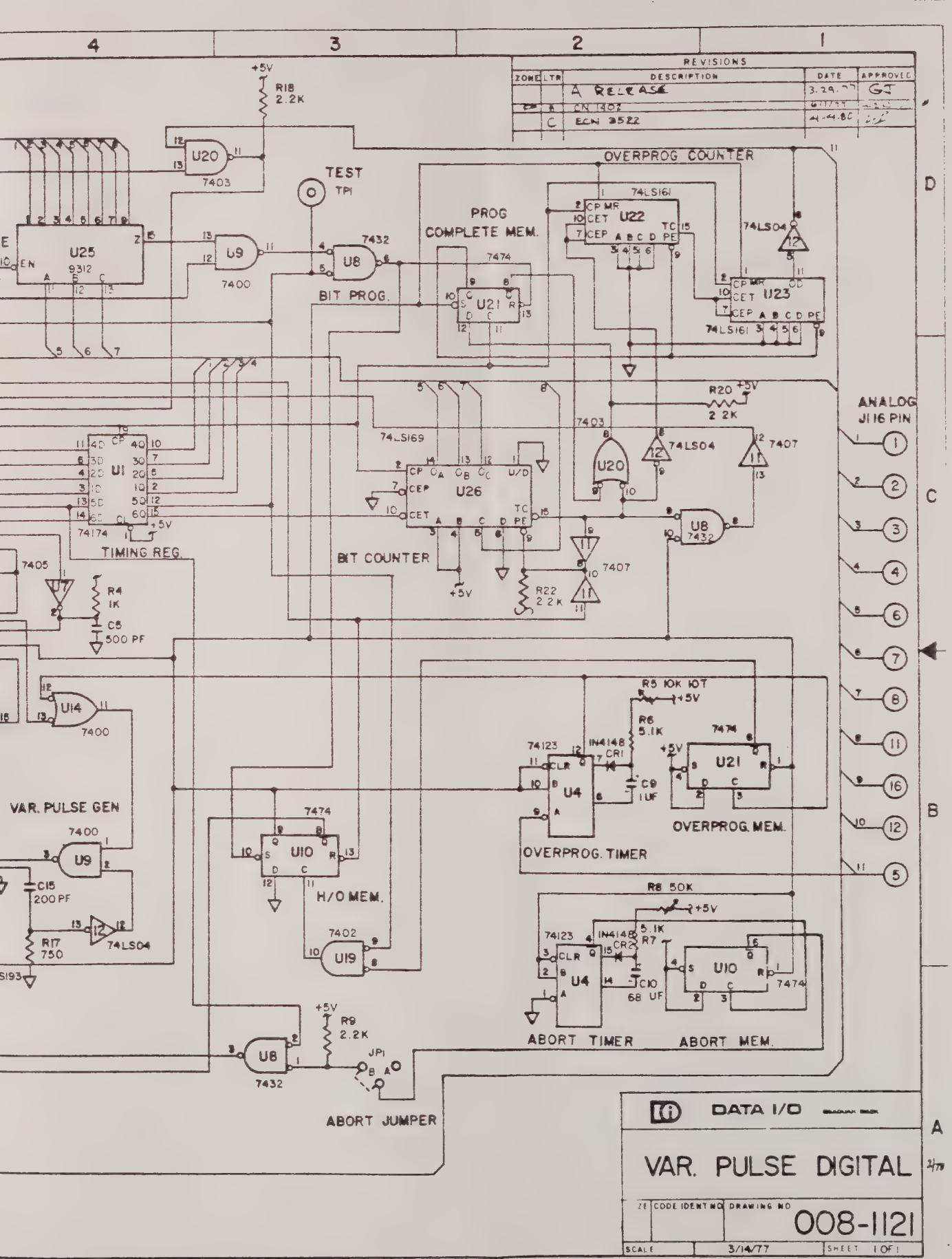
5.3.6 CHIP ENABLE SUPPLY

The Chip Enable Supply, upon digital card control, outputs TTL levels to CS2, a TTL "1" level to CS4 during read and a 10 volt level at 4 mA during Program/Verify. The TTL "1" level is provided to CS4 by the voltage divider action of R11 and R13 when U1 Pin 4 is low. The 10 volt level is supplied to CS4 through R13 and CR2.

SECTION 6
SCHEMATICS

008-1121	Var. Pulse Digital
008-1347-1	Intel Analog 2
010-1347-1	Truth Table
008-1072	Calibration Adapter


8
7
6
5
D
C
B
A
J6 MEU
DI1 DI2 DI3 DI4 DI5 DI6 DI7 DI8
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
M N P R S T U V
11 12 13 14 15 16 17 18
U24
9312
BIT DEC
CLK INH.
7407
PROG MEM.
+5V
7474
U13
R10
2.2K
STOP
22
U19
7406
U14
7400
PULSE SEQ.
WRITE
AA
7402
WRITE SEL.
PROG.
LL
C11
.001 UF
+5V
U5
74S124
R2
10K
10T
C1
47 PF
VERIFY
CLOCK
U8
7432
U3
74LS161
SEQ. COUNTER
R12
1K
C3
500 PF
U2
32 X 8
PROM
TIMING PROM
8 J
9 K
C18
22 UF
C2, C7, C8, C12, C13, C14, C16, C17,
.01
PROG PULSE COUNTER
74LS04
U17
U16
74LS169
R1
10K
10T
C4
47 PF
PROG PULSE
CLOCK
MOD 40 DECODE
U19
VER. A
19
U20
7403
VER. B
W
WRITE INH.
PF
7405
WRITE
OUTPUT
ENABLE
R9
2.2K
U6
C6
1UF
R3
10K
10T
RAMP CLOCK
U9
U18
U15
74LS193
R16
R15
R14
R13
JP2
RAMP COUNTER
R11
2.2K
READ
X
U14
7400
74LS04
READ INH.
RR
R23
2.2K
U19
7402
READ
READ OUTPUT
R21
2.2K
U13
7474
RAMP RATE MEM.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D
C
B
A
+5V
R18 2.2K
U20
7403
TEST
TP1
U25
9312
EN
U9
7400
U8
7432
BIT PROG.
PROG COMPLETE MEM.
7474
U21
OVERPROG COUNTER
74LS161
U22
U23
74LS04
74LS161
U1
74174
TIMING REG.
74LS169
U26
BIT COUNTER
R20 2.2K
7403
U20
74LS04
7407
U8
7432
R22 2.2K
7407
+5V
7405
R4 1K
C8 500 PF
U14
7400
VAR. PULSE GEN
7400
U9
C15 200 PF
R17 750
74LS04
R5 10K 10T
+5V
R6 5.1K
74123
IN4148 CR1
C9 1UF
U4
7474
U21
OVERPROG. MEM.
OVERPROG. TIMER
7474
U10
H/O MEM.
7402
U19
R8 50K
+5V
5.1K R7
74123
IN4148 CR2
C10 68 UF
U4
U10
7474
ABORT TIMER
ABORT MEM.
+5V
R9 2.2K
U8
7432
JP1
ABORT JUMPER
ANALOG J116 PIN
1
2
3
4
6
7
8
11
16
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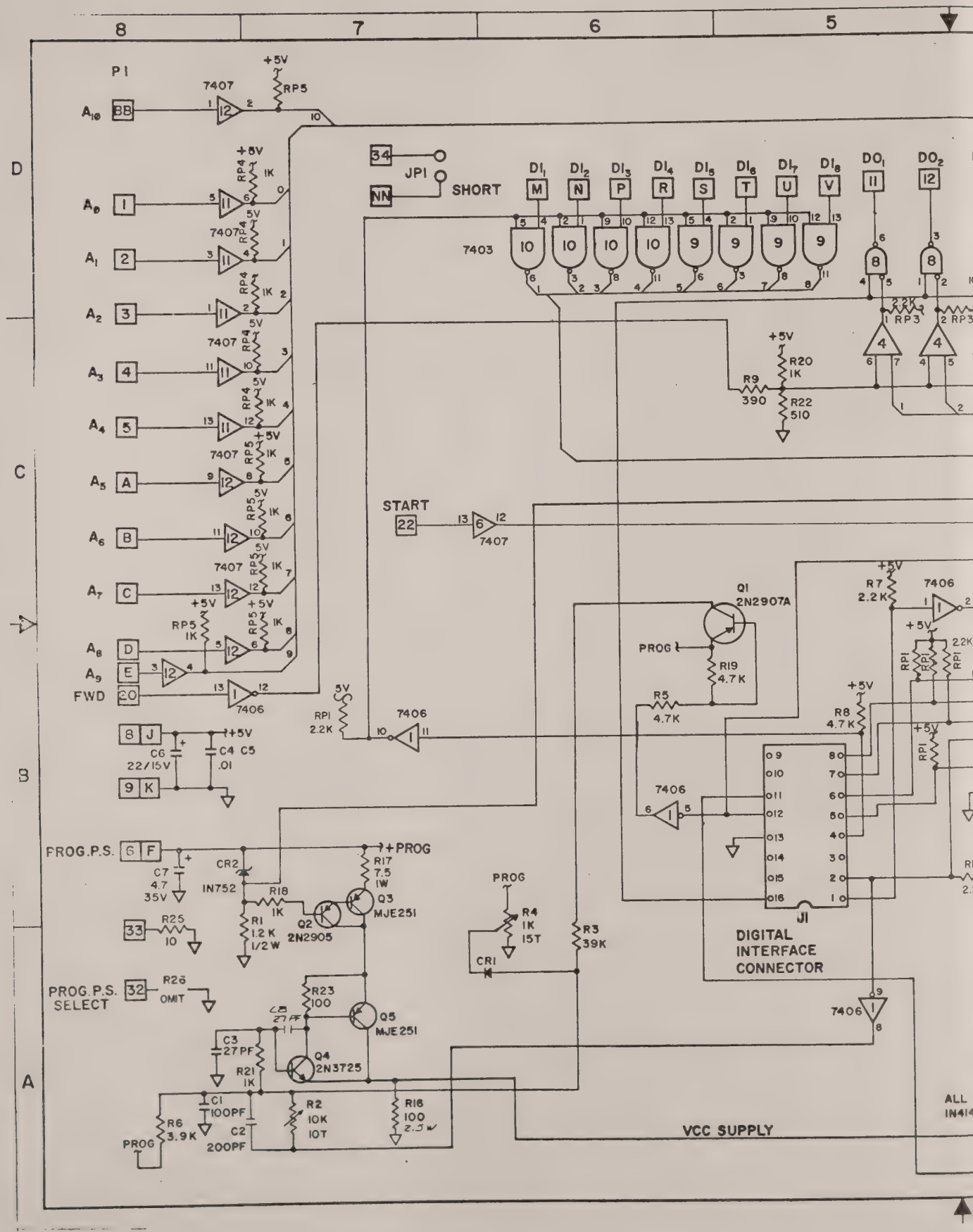
008-1121
SCALE
3/14/77
SHEET 1 OF 1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D
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DI2
DI3
DI4
DI5
DI6
DI7
DI8
M
N
P
R
S
T
U
V
7403
DO1
DO2
11
12
RP4
1K
RP3
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R20
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R9
390
R22
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A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
FWD
1
2
3
4
5
A
B
C
D
E
20
7406
START
22
Q1
2N2907A
PROG
R19
4.7K
R5
4.7K
R7
2.2K
R8
4.7K
RPI
2.2K
C6
22/15V
C4 C5
.01
8
J
9
K
DIGITAL
INTERFACE
CONNECTOR
J1
PROG.P.S.
6
F
C7
4.7
35V
CR2
IN752
R18
1K
R1
1.2K
1/2W
Q2
2N2905
R17
7.5
1W
Q3
MJE251
+PROG
33
R25
10
PROG
R4
1K
15T
CR1
R3
39K
PROG.P.S.
SELECT
32
R26
OMIT
R23
100
Q5
MJE251
C3
27PF
R21
1K
Q4
2N3725
C1
100PF
C2
200PF
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10T
R6
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R16
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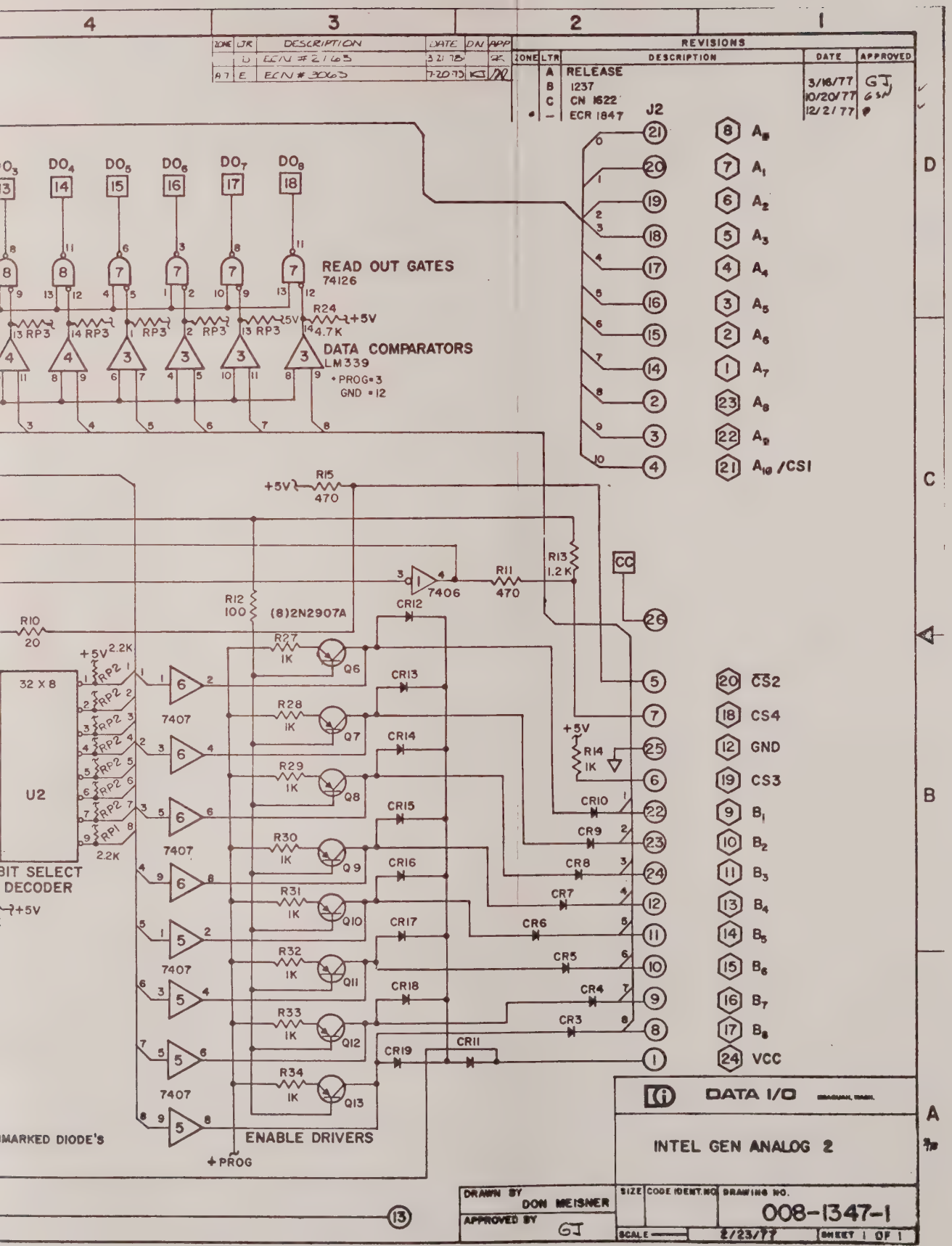
2.5W
VCC SUPPLY
ALL
IN414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4.7K
+5V
RP3
R15
470
R11
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R13
1.2K
R12
100
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R10
20
2.2K
RP2
RP1
32 X 8
U2
BIT SELECT
DECODER
7407
R27
R28
R29
R30
R31
R32
R33
R34
1K
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR11
CR10
CR9
CR8
CR7
CR6
CR5
CR4
CR3
R14
CC
26
5
7
25
6
22
23
24
12
11
10
9
8
1
20 CS2
18 CS4
12 GND
19 CS3
9 B1
10 B2
11 B3
13 B4
14 B5
15 B6
16 B7
17 B8
24 VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10 /CS1
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ENABLE DRIVERS
+PROG
DATA I/O
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DRAWN BY DON MEISNER
APPROVED BY GJ
SIZE | CODE IDENT. NO. | DRAWING NO. 008-1347-1
SCALE | 2/23/77 | SHEET 1 OF 1
13

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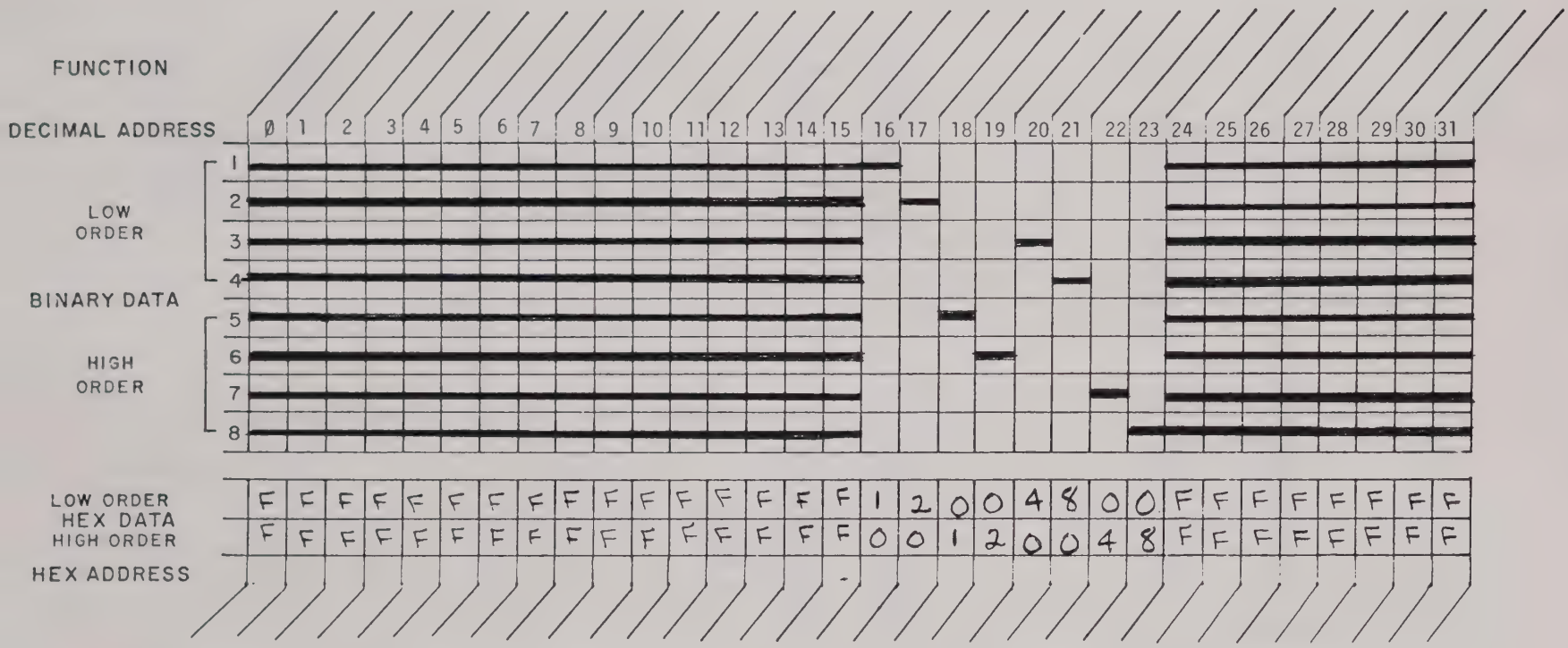
3/77	A	RELEASE	GJ	GJ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BINARY DATA
HIGH ORDER
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2
3
4
5
6
7
8
LOW ORDER HEX DATA
HIGH ORDER
HEX ADDRESS
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F F F F F F F F F F F F F F F F 0 0 1 2 0 0 4 8 F F F F F F F F

NOTES

1. "1" = HIGH.
2. "1" = PAPER TAPE HOLE.
3. FOR V_{OL} PROGRAMMING PROMS, INVERT SWITCH ON READER DRIVER CARD MUST BE INVERT.
4. ALL UNDEFINED ADDRESS LOCATIONS MUST BE ALL "1's", (HIGHS).

PROM LABEL

2 -1347-1A

"U" LOCATION
CARD NUMBER
DASH AND REVISION

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.			
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			APPROVED BY	
FRACTIONAL ±	TITLE: INTEL GENERIC #2			
ANGULAR ±	DATE	DRAWING NUMBER 010-1347	SHT 1/1	

DATE	SYM	REVISION RECORD	DR	CK
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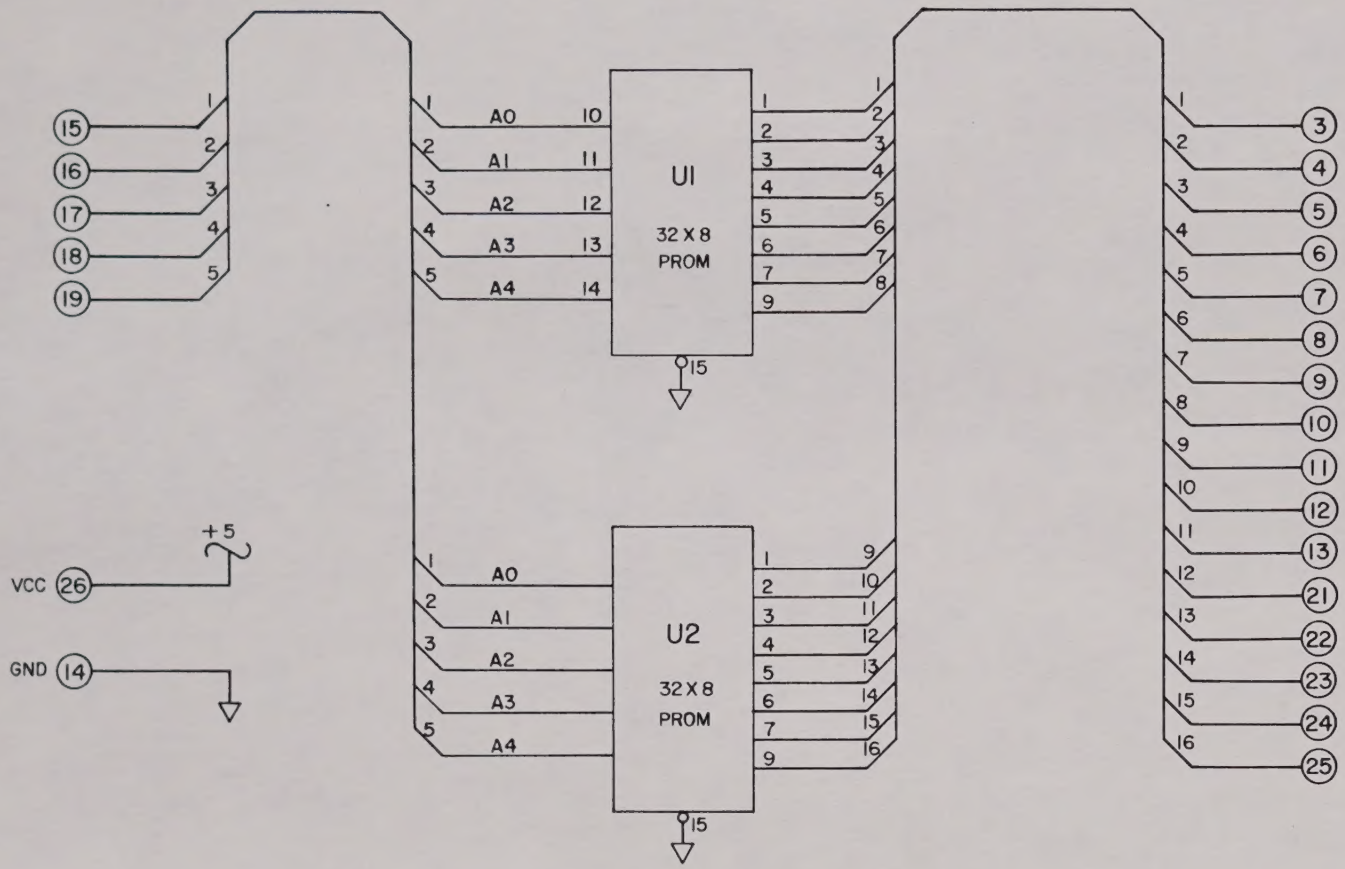

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
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			APPROVED BY
FRACTIONAL .	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		
ANGULAR .	DATE 10-15-75	DRAWING NUMBER 008-1072	

DATA I/O

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